PATENT ABSTRACTS OF JAPAN

(11)Publication number : 07-066207
(43)Date of publication of application : 10.03.1995

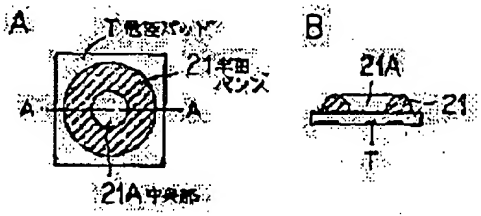
(51)Int.Cl. H01L 21/321
H01L 21/60
H05K 3/34

(21)Application number : 05-209767
(22)Date of filing : 24.08.1993

(71)Applicant : SONY CORP
(72)Inventor : ISHIKAWA NATSUYA

(54) SURFACE MOUNT DEVICE, MANUFACTURE THEREOF, AND SOLDERING METHOD

(57)Abstract:
PURPOSE: To solder a surface mount device to a circuit board without causing defective bonds by giving its electrodes solder bumps with a recess in the center so that they can seat on conductive projections on the board to correctly position the device.
CONSTITUTION: A surface mount device has electrodes T each provided with a solder bump 21 having a recess in the center. For example, a ring-shaped solder bump 21 with a recess 21A in the center is formed on the electrode pad of a surface mount device, such as a flip chip IC. Such a device is mounted on a circuit board in such a manner that the recessed bumps seat on conductive projections on the board. Then, the surface mount device is soldered to the board by heating.



LEGAL STATUS

[Date of request for examination]	16.12.1999
[Date of sending the examiner's decision of rejection]	
[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]	
[Date of final disposal for application]	
[Patent number]	3263875
[Date of registration]	28.12.2001
[Number of appeal against examiner's decision of rejection]	
[Date of requesting appeal against examiner's decision of rejection]	
[Date of extinction of right]	

CLAIMS

[Claim(s)]

[Claim 1] Surface mount mold electronic parts with which the cross section was equipped with the solder bump of a concave or trapezoidal shape on the front face of the electrode of surface mount mold electronic parts.

[Claim 2] The soldering approach of the surface mount mold electronic parts characterized by arranging and for the solder bump's said crevice or the trapezoid section coalescing the surface mount mold electronic parts of claim 1 so that the cross section formed in the electrode of an electrical circuit wiring substrate may sit on the heights of a convex conductive land, and heat-treating both in the state of the coalesce after that, and soldering said surface mount mold electronic parts to an electrical circuit wiring substrate.

[Claim 3] Surface mount mold electronic parts characterized by the thing of the solder bump formed on the front face of the electrode of surface mount mold electronic parts for which the center section is filled up with resin at least.

[Claim 4] The manufacture approach of the surface mount mold electronic parts characterized by making solder adhere and forming a solder bump on the front face of the electrode of the electrode of surface mount mold electronic parts which covers a center-section front face with insulating resin at least, and is not covered with this insulating resin.

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Industrial Application] This invention relates to the soldering approach at structure and its manufacture approach list of the solder bump formed in the electrode of surface mount mold electronic parts, such as for example, flip chip mold semiconductor integrated circuit equipment (it is only hereafter described as "the flip chip mold IC") or a miniature switch, and a connector of a ** pitch.

[0002]

[Description of the Prior Art] The situation at the time of carrying out the surface mount of the structure of the surface mount mold electronic parts of the conventional technique, for example,

the electrode of the flip chip mold IC, and such a flip chip mold IC to an electrical circuit wiring substrate (it only being hereafter described as a "substrate") is explained using drawing 7 . Drawing 7 is the side elevation having shown the condition at the time of carrying out the surface mount of the structure of the electrode of the flip chip mold IC of the conventional technique, and its flip chip mold IC to a substrate.

[0003] This seed substrate 1 of the conventional technique is formed by electric insulation material, such as ceramic material, such as organic material, such as a glass epoxy resin, and an alumina, and the electrical circuit consists of conductive lands 2 which projected a little on that front face, and were formed in two or more conductive wiring sections and those edges.

[0004]

[Problem(s) to be Solved by the Invention] A place high-density-integrates surface mount mold electronic parts, such as the recently and flip chip mold IC, it comes to be miniaturized, and electrodes increase in number along with it, and those electrodes are formed into a ** pitch. Moreover, said conductive land of the substrate which mounts such surface mount mold electronic parts also came to be formed into the ** pitch.

[0005] Although flux is applied to the front face of the solder 3 put on the conductive land 2 and he is trying to carry the flip chip mold IC 10 in the front face when it mounts the flip chip mold IC 10 formed into the ** pitch in a substrate 1, it can often see that the flip chip type IC 10 of solder bump 11 slips down between the conductive lands 2, and causes poor mounting by flow of flux as shown in drawing 7 . Said flip chip type IC 10 of solder bump 11 is having convex structure, and the solder 3 on said conductive land 2 had also become convex structure, and these causes carried said convex solder bump 11 on this convex solder 3, and were a thing resulting from what you are going to make connect. This invention makes it a technical problem to solve such poor mounting.

[0006]

[Means for Solving the Problem] So, in this invention, the solder bump was formed on the electrode surface of the surface mount mold IC, and that cross-section configuration was made into a concave or trapezoidal shape. And it has arranged and these solder bump's crevice or the trapezoid section coalesced so that the cross section formed in the substrate might sit on the heights of a convex conductive land, both were heat-treated in the state of the coalesce after that, and the approach of soldering said surface mount mold IC to the substrate was taken.

[0007] Moreover, such a solder bump formed by making solder adhere on the

front face of the electrode of the electrode of surface mount mold electronic parts which covers a center section front face with insulating resin at least, and is not covered with this insulating resin. Said technical problem was solved by taking the soldering approach in the above surface mount mold electronic parts' structure and its manufacture approach list of a solder bump.

[0008]

[Function] Therefore, since the solder bump of the concave of these surface mount mold electronic parts or trapezoidal shape becomes easy to sit on the convex conductive land of a substrate, the solder bump of these surface mount mold electronic parts does not slip down between the conductive lands of a substrate.

[0009]

[Example] First, drawing 1 thru/or drawing 6 are used for the structure and its manufacture approach list of surface mount mold electronic parts of this invention, and the example of the soldering approach is explained to them. Drawing 1 shows the example of the structure of the solder bump of the surface mount mold electronic parts of this invention. The top view and this drawing B of this drawing A are cross-section side elevations on the A-A line of this drawing A. Drawing 2 is the top view having shown the structure of the example of others of the solder bump of the surface mount mold electronic parts of this invention. Those with process drawing for drawing 3 to explain the manufacture approach of the solder bump of the surface mount mold electronic parts of this invention shown in drawing 1 , Drawing 4 shows the soldering approach which carries out the surface mount of the surface mount mold electronic parts of this invention to a substrate. This drawing A is a cross-section side elevation having shown the condition of having laid the surface mount mold electronic parts of this invention in the substrate. Those with a cross-section side elevation, as for this drawing B, surface mount mold electronic parts indicated the condition of having been soldered to the substrate to be, Drawing 5 shows the surface mount mold switch of this invention. This drawing A That perspective view, The top view of the structure of the conductive terminal and this drawing C of this drawing B are cross-section side elevations on the A-A line of this drawing B. And drawing 6 shows the soldering approach which carries out the surface mount of the surface mount mold switch shown in drawing 5 to a substrate. For this drawing A, this drawing B is cross-section side elevation **** which showed the condition that were the perspective view having shown the condition of laying the surface mount mold switch of this invention in the

substrate, and the surface mount mold switch was soldered to the substrate. In addition, the same sign is given to the same part as the surface mount mold electronic parts of the conventional technique etc., and explanation of those parts is omitted.

[0010] The solder bump 21 of the surface mount mold electronic parts of this invention of the example shown in drawing 1 is formed in the front face of the electrode pad T of those surface mount mold electronic parts at the structure which heaped up solder annularly so that that center-section 21A might become a concave.

[0011] A solder bump's structure where the effectiveness the structure of the solder bump 21 of the example shown in drawing 2 at drawing 1, the same, or almost same was acquired was mentioned. The solder bumps 22 of this drawing A are the four corners of the front face of the electrode pad T, and are the example which heaped up solder 22a in the shape of a semi-sphere, and formed the hollow by center-section 22A of these four solder 22a. The solder bumps 23 of this drawing B are the four corners of the front face of the electrode pad T, and are the example which heaped up solder 23a in the shape of a pyramid, and formed the hollow by center-section 23A of these four solder 23a. The solder bump 24 of this drawing C is the example which heaped up solder 24a and formed the hollow by center-section 24A of solder 24a of these neighborhoods along with the neighborhood of the front face of the electrode pad T. And the solder bump 25 of this drawing D is the example which formed the hollow by pars intermedia 25A which solder 25a is heaped up in parallel along with two sides of the front face of the electrode pad T, and solder of these two sides 25a faces.

[0012] Next, the flip chip mold IC is mentioned as an example as surface mount mold electronic parts, and how to form the annular solder bump 21 who showed the electrode pad at drawing 1 is explained using drawing 3. First, it is SiO2, as were shown in the process of this drawing A, and the electrode pad T of the flip chip mold IC 10 is formed with the aluminum of the square whose die length La of one side is 110 micrometers and it leaves with an one-side square [100-micrometer square] opening for the front face of the electrode pad T. It covers by the insulator layer 30.

[0013] Next, as shown in this drawing B, patterning of the insulating resin film 31 of outer-diameter 90micrometerphi and a duplex circle with a bore [phi] of 30 micrometers is carried out for the electrode pad T top using photosensitive polyimide. Next, as shown in this drawing C, the 1st layer of the thin film 32 of Cr and the 2nd layer nickel is formed to the flip chip mold IC10 whole using a sputtering system. Next, as

shown in this drawing D, patterning of the two-layer film 32A of Cr and nickel is carried out near electrode pad T of the flip chip mold IC 10 using the photolithography method using a photosensitive resist. In this case, patterning is carried out so that most insulating resin film 31 which exists at the core of the electrode pad T may be exposed.

[0014] Next, at the process of drawing D, as shown in this drawing E, patterning is carried out using the photolithography method using the thick-film photosensitivity resist 33 so that the great portion of Cr which carried out patterning, and nickel film 32A may be exposed. In this case, all the parts by which Cr and nickel film 32A are not formed are covered by the thick-film sensitization resist 33. Following this process, as shown in this drawing F using the vacuum evaporation system from all the front faces of said thick-film sensitization resist 33, solder 34 is formed.

[0015] Next, as shown in this drawing G, the thick-film sensitization resist 33 formed at the process of drawing E is removed using exfoliation liquid. At this time, the solder 34 deposited on the thick-film sensitization resist 33 is also removed by coincidence. And oven is used by the following final process, the components made from the process of drawing G are heated, and solder 34 is fused.

[0016] In this case, if there is little thickness of the solder 34 formed at the process of drawing G, as shown in drawing H Solder 34 does not accumulate on the insulating resin film 31 prepared in the core of the electrode pad T of the flip chip mold IC 10. If the thickness of the solder 34 which the flip chip mold IC 40 of this invention with which the solder bump 21 did the concave form was obtained, and was formed in drawing G is thick, as shown in drawing I, flip chip mold IC40A of this invention of the shape of a base where the front face of solder bump 21A is almost even can be obtained. The solder bump 21 of this invention who showed drawing 1 can be formed on each electrode pad T of the flip chip mold IC 10 through the above processes.

[0017] Next, the surface mount approach to the substrate 1 of the flip chip mold IC 40 of this invention is explained using drawing 4 . First, after putting solder 3 on the conductive land 2 formed in the substrate 1 and applying flux to the front face of that solder 3, the flip chip mold IC 40 of **** for flip chip bonders and this invention is laid in that front face (drawing 4 A).

[0018] In this case, when the flip chip mold IC 40 of drawing 3 H is laid in the conductive land 2, it can prevent the flip chip mold IC 40 shifting from the conductive land 2 by arranging and coalescing so that that concave solder

bump 21 may sit on the convex solder 3 on the conductive land 2 (drawing 4 A). Moreover, when flip chip mold IC40A as shown in drawing K is laid on the solder 3 of the conductive land 2, there is no said about 21 solder bump gap prevention effectiveness by arranging and coalescing so that solder bump 21A of the shape of the base may sit on the convex solder 3 on the conductive land 2, but if it compares with the conventional convex electrode and connection of a convex conductive land, Haruka will get ** which mitigates a gap.

[0019] If oven is used and both are finally heat-treated in the state of this coalesce, as shown in drawing 4 B, said electrode pad T and conductive land 2 can be joined with solder, and the flip chip mold 40 and ICs 40A can be soldered to a substrate 1.

[0020] Next, a surface mount mold switch (it is only hereafter described as a "switch") is taken and mentioned as other electronic parts of surface mount mold electronic parts, and the 2nd example is explained using drawing 5 and drawing 6 .

[0021] In drawing 5 , the sign 50 has pointed out the switch of this invention and this switch 50 is equipped with two conductive terminals 51. As shown in these drawings B and C, the concave solder bump 53 by whom the center section became depressed is formed in these conductive terminals 51. This solder bump 53 can apply thinly the resin film 52, such as an epoxy resin and silicone resin, to the center section of the electrode pad T, and can form by making this electrode pad T dip and adhere to solder after that.

[0022] Like the flip chip mold IC 40 of the 1st aforementioned example, since the crevice is formed in the solder bump 53, the switch 50 of such structure is easy coming to sit on the heights of the solder 3 of the conductive land 2 formed in the substrate 1, and stops being able to shift easily. Therefore, it will be tacking carried out in this condition, the conductive land 2 of the solder formed in the conductive terminal 51 and substrate 1 of a switch 50 by carrying out a reflow of the substrate 1 in this condition is soldered, and it can connect (drawing 6 B). In addition, a sign 54 points out the knob of a switch 50.

[0023]

[Effect of the Invention] Even if it will do the activity which carries out the surface mount of the electronic parts on a substrate, and makes solder connection of the conductive land of the electrode of electronic parts, and a substrate if the surface mount mold electronic parts of this invention are used as explained above, it can connect without a solder bump and a conductive land shifting, and reliable soldering which does not cause poor soldering can be performed.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] The example of the structure of the solder bump of the surface mount mold electronic parts of this invention is shown, and that top view and this drawing B of this drawing A are cross-section side elevations on the A-A line of this drawing A.

[Drawing 2] It is the top view having shown the structure of the example of others of the solder bump of the surface mount mold electronic parts of this invention.

[Drawing 3] It is process drawing for explaining the manufacture approach of the solder bump of the surface mount mold electronic parts of this invention shown in drawing 1 .

[Drawing 4] The soldering approach which carries out the surface mount of the surface mount mold electronic parts of this invention to a substrate is shown, this drawing A is a cross-section side elevation having shown the condition of having laid the surface mount mold electronic parts of this invention in the substrate, and this drawing B is a cross-section side elevation having shown the condition that surface mount mold electronic parts were soldered to the substrate.

[Drawing 5] The surface mount mold switch of this invention is shown, and this drawing A is [the top view of the structure of that conductive terminal and this drawing C of that perspective view and this drawing B] cross-section side elevations on the A-A line of this drawing B.

[Drawing 6] The soldering approach which carries out the surface mount of the surface mount mold switch shown in drawing 5 to a substrate is shown, this drawing A is a perspective view having shown the condition of laying the surface mount mold switch of this invention in the substrate, and this drawing B is a cross-section side elevation having shown the condition that the surface mount mold switch was soldered to the substrate.

[Drawing 7] It is the side elevation having shown the condition at the time of carrying out the surface mount of the structure of the electrode of the flip chip mold IC of the conventional technique, and its flip chip mold IC to a substrate.

[Description of Notations]

T Electrode pad

1 Electrical Circuit Wiring Substrate (Substrate)

2 Conductive Land

3 Solder

21 Solder Bump of Cross-Section Concave

21A The solder bump of cross-section trapezoidal shape

31 Insulating Resin Film

34 Solder

40 Flip Chip Mold IC Equipped with Solder Bump of Cross-Section Concave

40A The flip chip mold IC equipped with

the solder bump of cross-section trapezoidal shape

50 Surface Mount Mold Switch

51 Conductive Terminal

52 Resin Film

53 Solder Bump of Cross-Section Concave

(19)日本国特許庁（ＪＰ）　(12)公開特許公報（A）　(11)特許出願公開番号

特開平7－66207

(43)公開日　平成７年(1995)３月10日

(51)Int.Cl.[6]		識別記号	庁内整理番号	FI	技術表示箇所
H01L	21/321				
	21/60	311 S	6918－4M		
H05K	3/34		7128－4E		
			9168－4M	H01L 21/92	C
			9168－4M		F

審査請求　未請求　請求項の数４　ＯＬ　（全５頁）

(21)出願番号　特願平5－209767

(22)出願日　平成５年(1993)８月24日

(71)出願人　000002185
ソニー株式会社
東京都品川区北品川６丁目７番35号

(72)発明者　石川　夏也
東京都品川区北品川６丁目７番35号ソニー株式会社内

(74)代理人　弁理士　高橋　光男

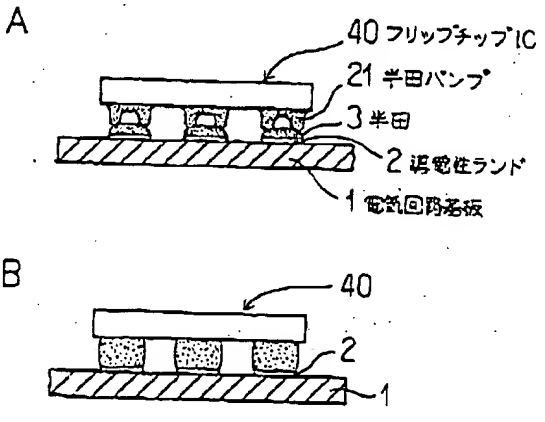
(54)【発明の名称】　表面実装型電子部品及びその製造方法並びに半田付け方法

(57)【要約】　（修正有）

【目的】　表面実装型電子部品を電気回路配線基板に確実に表面実装すること。

【構成】　フリップチップ型ＩＣ４０の電極パッドＴの表面上に半田バンプ２１を形成し、その断面形状を凹状または台形状とした。このような半田バンプ２１は、電極パッドＴの少なくとも中央部表面を絶縁樹脂膜３１で被覆し、この絶縁樹脂３１で被覆されていない電極パッドＴの表面上に半田３４を付着させることにより形成している。

【効果】　この表面実装型電子部品の凹状または台形状の半田バンプが基板の凸状の導電性ランドに座り易くなるので、導電性ランド間にずり落ちることがなく、半田付け不良を起こさない。



1

【特許請求の範囲】

【請求項1】　表面実装型電子部品の電極の表面上に、断面が凹状または台形状の半田バンプを備えた表面実装型電子部品。

【請求項2】　請求項1の表面実装型電子部品を、その半田バンプの前記凹部または台形部が、電気回路配線基板の電極に形成された断面が凸状の導電性ランドのその凸部に座るように配置、合体し、その後、その合体状態で両者を加熱処理して、前記表面実装型電子部品を電気回路配線基板に半田付けすることを特徴とする表面実装型電子部品の半田付け方法。

【請求項3】　表面実装型電子部品の電極の表面上に形成された半田バンプの少なくとも中央部に樹脂が充填されていることを特徴とする表面実装型電子部品。

【請求項4】　表面実装型電子部品の電極の少なくとも中央部表面を絶縁樹脂で被覆し、この絶縁樹脂で被覆されていない電極の表面上に半田を付着させて半田バンプを形成することを特徴とする表面実装型電子部品の製造方法。

【発明の詳細な説明】

【0001】

【産業上の利用分野】この発明は、例えば、フリップチップ型半導体集積回路装置（以下、単に「フリップチップ型ＩＣ」と記す）、或いは小型スイッチや狭ピッチのコネクターなどの表面実装型電子部品の電極に形成された半田バンプの構造及びその製造方法並びに半田付け方法に関するものである。

【0002】

【従来の技術】従来技術の表面実装型電子部品、例えば、フリップチップ型ＩＣの電極の構造及びそのようなフリップチップ型ＩＣを電気回路配線基板（以下、単に「基板」と記す）に表面実装した場合の様子を図7を用いて説明する。図7は従来技術のフリップチップ型ＩＣの電極の構造及びそのフリップチップ型ＩＣを基板に表面実装した場合の状態を示した側面図である。

【0003】従来技術のこの種基板1は、ガラスエポキシ樹脂などの有機材やアルミナなどのセラミック材など、電気絶縁材で形成されており、その表面にやや突出して複数の導電性配線部とそれらの端部に形成された導電性ランド2とで電気回路が構成されている。

【0004】

【発明が解決しようとする課題】所が、最近、フリップチップ型ＩＣなどの表面実装型電子部品は高密度集積化、小型化されるようになり、それにつれ電極が多くなり、そしてそれらの電極が狭ピッチ化されるようになっている。また、このような表面実装型電子部品を実装する基板の前記導電性ランドも狭ピッチ化されるようになった。

【0005】狭ピッチ化されたフリップチップ型ＩＣ10を基板1に実装する場合は、導電性ランド2に被着した半田3の表面にフラックスを塗布し、その表面にフリップチップ型ＩＣ10を搭載するようにしているが、フラックスの流動により、図7に示したように、そのフリップチップ型ＩＣ10の半田バンプ11が導電性ランド2間にずり落ちてしまい、実装不良を起こすことがしばしば見受けられる。これらの原因は、前記フリップチップ型ＩＣ10の半田バンプ11が凸状の構造をしており、また前記導電性ランド2上の半田3も凸状の構造になっており、この凸状の半田3の上に前記凸状の半田バンプ11を載せ、接続させようとすることに起因するものであった。この発明は、このような実装不良を解決することを課題とするものである。

2

【0006】

【課題を解決するための手段】それ故、この発明では、表面実装型ＩＣの電極表面上に半田バンプを形成し、その断面形状を凹状または台形状とした。そして、それら半田バンプの凹部または台形部が、基板に形成された断面が凸状の導電性ランドのその凸部に座るように配置、合体し、その後、その合体状態で両者を加熱処理して、前記表面実装型ＩＣをその基板に半田付けする方法を採った。

【0007】また、このような半田バンプは、表面実装型電子部品の電極の少なくとも中央部表面を絶縁樹脂で被覆し、この絶縁樹脂で被覆されていない電極の表面上に半田を付着させることにより形成した。以上のような表面実装型電子部品の半田バンプの構造及びその製造方法並びに半田付け方法を採ることにより、前記課題を解決した。

【0008】

【作用】従って、この表面実装型電子部品の凹状または台形状の半田バンプが基板の凸状の導電性ランドに座り易くなるので、この表面実装型電子部品の半田バンプが基板の導電性ランド間にずり落ちることがない。

【0009】

【実施例】先ず、この発明の表面実装型電子部品の構造及びその製造方法並びに半田付け方法の実施例を図1乃至図6を用いて説明する。図1はこの発明の表面実装型電子部品の半田バンプの構造の実施例を示していて、同図Ａはその平面図、同図Ｂは同図ＡのＡ－Ａ線上の断面側面図であり、図2はこの発明の表面実装型電子部品の半田バンプのその他の実施例の構造を示した平面図であり、図3は図1に示したこの発明の表面実装型電子部品の半田バンプの製造方法を説明するための工程図あり、図4はこの発明の表面実装型電子部品を基板に表面実装する半田付け方法を示していて、同図Ａは基板にこの発明の表面実装型電子部品を載置した状態を示した断面側面図であり、同図Ｂは表面実装型電子部品が基板に半田付けされた状態を示した断面側面図あり、図5はこの発明の表面実装型スイッチを示していて、同図Ａはその斜視図、同図Ｂはその導電性端子の構造の平面図、同図Ｃ

は同図BのA－A線上の断面側面図であり、そして図6は図5に示した表面実装型スイッチを基板に表面実装する半田付け方法を示していて、同図Aは基板にこの発明の表面実装型スイッチを載置する状態を示した斜視図であり、同図Bは表面実装型スイッチが基板に半田付けされた状態を示した断面側面図ある。なお、従来技術の表面実装型電子部品などと同一の部分には同一の符号を付して、それらの部分の説明を省略する。

【0010】図1に示した実施例のこの発明の表面実装型電子部品の半田バンプ21は、その表面実装型電子部品の電極パッドTの表面に、その中央部21Aが凹状になるよう半田を環状に盛り上げた構造に形成されている。

【0011】図2に、図1に示した実施例の半田バンプ21の構造と同一、またはほぼ同一の効果が得られる半田バンプの構造を挙げた。同図Aの半田バンプ22は電極パッドTの表面の四隅で、半田22aを半球状に盛り上げ、それら4個の半田22aの中央部22Aで窪みを形成した実施例である。同図Bの半田バンプ23は電極パッドTの表面の四隅で、半田23aを角錐状に盛り上げ、それら4個の半田23aの中央部23Aで窪みを形成した実施例である。　同図Cの半田バンプ24は電極パッドTの表面の四辺に沿って、半田24aを盛り上げ、それら四辺の半田24aの中央部24Aで窪みを形成した実施例である。そして、同図Dの半田バンプ25は電極パッドTの表面の二辺に沿って平行に、半田25aを盛り上げ、それら二辺の半田25aが相対する中間部25Aで窪みを形成した実施例である。

【0012】次に、表面実装型電子部品としてフリップチップ型ICを実施例として挙げ、その電極パッドに、図1に示した環状の半田バンプ21を形成する方法を図3を用いて説明する。先ず、同図Aの工程に示したように、フリップチップ型IC10の電極パッドTは、例えば、一辺の長さLaが110μmの正方形のアルミで形成されており、その電極パッドTの表面を一辺100μmの正方形の開口部を残すようにしてSiO_2の絶縁膜30で覆う。

【0013】次に、同図Bに示したように、感光性ポリイミドを用いて電極パッドT上を外径90μmφ、内径30μmφの二重円の絶縁樹脂膜31をパターニングする。次に、同図Cに示したように、スパッタ装置を用いて、第1層Cr、第2層Niの薄膜32をフリップチップ型IC10全体に成膜する。次に、同図Dに示したように、感光性レジストを用いたフォトリソグラフィー法を用いて、フリップチップ型IC10の電極パッドT付近にCr、Niの2層膜32Aをパターニングする。この場合、電極パッドTの中心にある絶縁樹脂膜31の大部分が露出するようにパターニングする。

【0014】次に、同図Eに示したように、図Dの工程でパターニングしたCr、Ni膜32Aの大部分を露出させるように厚膜感光性レジスト33を用いたフォトリソグラフィー法を用いてパターニングする。この場合、Cr、Ni膜32Aが成膜されていない部分は、全て厚膜感光レジスト33で覆われている。この工程に続いて、前記厚膜感光レジスト33の全表面から真空蒸着装置を用いて、同図Fに示したように、半田34を成膜する。

【0015】次に、同図Gに示したように、図Eの工程で形成した厚膜感光レジスト33を剥離液を用いて除去する。この時、厚膜感光レジスト33上に堆積した半田34も同時に除去される。そして、次の最終工程でオーブンを使用し、図Gの工程で作られた部品を加熱し、半田34を溶融する。

【0016】この場合、図Gの工程で形成された半田34の膜厚が少なければ、図Hに示したように、フリップチップ型IC10の電極パッドTの中心に設けられた絶縁樹脂膜31上に半田34が堆積せず、半田バンプ21が凹状の形をしたこの発明のフリップチップ型IC40が得られ、また、図Gで形成された半田34の膜厚が厚ければ、図Iに示したように、半田バンプ21Aの表面がほぼ平らな台状のこの発明のフリップチップ型IC40Aを得ることができる。以上のような工程を経て、図1に示したこの発明の半田バンプ21をフリップチップ型IC10の各電極パッドT上に形成することができる。

【0017】次に、図4を用いて、この発明のフリップチップ型IC40の基板1への表面実装方法を説明する。先ず、基板1に形成された導電性ランド2上に半田3を被着し、その半田3の表面にフラックスを塗布した後、その表面にフリップチップボンダー用いて、この発明のフリップチップ型IC40を載置する（図4A）。

【0018】この場合、図3Hのフリップチップ型IC40を導電性ランド2に載置した時は、その凹状の半田バンプ21が導電性ランド2上の凸状の半田3に座るように配置、合体することにより、フリップチップ型IC40が導電性ランド2からずれるのを防ぐことができる（図4A）。また、図Kのようなフリップチップ型IC40Aを導電性ランド2の半田3上に載置した時は、その台状の半田バンプ21Aが導電性ランド2上の凸状の半田3に座るように配置、合体することにより、前記半田バンプ21程のずれ防止効果はないが、従来の凸状電極と凸状の導電性ランドの接続と比較すれば遙にずれを軽減するこができる。

【0019】最後に、オーブンを用い、この合体状態で両者を加熱処理すると、図4Bに示したように、前記電極パッドTと導電性ランド2とを半田接合させることができ、フリップチップ型IC40、40Aを基板1に半田付けできる。

【0020】次に、表面実装型電子部品の他の電子部品として、表面実装型スイッチ（以下、単に「スイッチ」

5

と記す）を採り挙げ、図5及び図6を用いて、第2の実施例を説明する。

【0021】図5において、符号50はこの発明のスイッチを指しており、このスイッチ50は2個の導電性端子51を備えている。これらの導電性端子51には、同図B、Cに示したように、中央部が窪んだ凹状の半田バンプ53が形成されている。この半田バンプ53は電極パッドTの中央部にエポキシ樹脂やシリコーン樹脂などの樹脂膜52を薄く塗布し、その後、この電極パッドTを半田にディップし、付着させることにより形成することができる。

【0022】このような構造のスイッチ50は、前記の第1の実施例のフリップチップ型IC40と同様に、その半田バンプ53に凹部が形成されているので、基板1に形成された導電性ランド2の半田3の凸部に座り良くなり、ずれ難くなる。従って、この状態で仮止めされた状態になり、この状態で基板1をリフローすることによりスイッチ50の導電性端子51と基板1に形成された半田の導電性ランド2とが半田付けされ、接続することができる（図6B）。なお、符号54はスイッチ50の摘みを指す。

【0023】

【発明の効果】以上説明したように、この発明の表面実装型電子部品を用いると、基板上に電子部品を表面実装し、電子部品の電極と基板の導電性ランドを半田接続する作業を行なっても、半田バンプと導電性ランドとがずれることなく接続することができ、半田付け不良を起こさない、信頼性の高い半田付けを行うことができる。

【図面の簡単な説明】

【図1】　この発明の表面実装型電子部品の半田バンプの構造の実施例を示していて、同図Aはその平面図、同図Bは同図AのA－A線上の断面側面図である。

【図2】　この発明の表面実装型電子部品の半田バンプのその他の実施例の構造を示した平面図である。

【図3】　図1に示したこの発明の表面実装型電子部品の半田バンプの製造方法を説明するための工程図である。

6

【図4】　この発明の表面実装型電子部品を基板に表面実装する半田付け方法を示していて、同図Aは基板にこの発明の表面実装型電子部品を載置した状態を示した断面側面図であり、同図Bは表面実装型電子部品が基板に半田付けされた状態を示した断面側面図である。

【図5】　この発明の表面実装型スイッチを示していて、同図Aはその斜視図、同図Bはその導電性端子の構造の平面図、同図Cは同図BのA－A線上の断面側面図である。

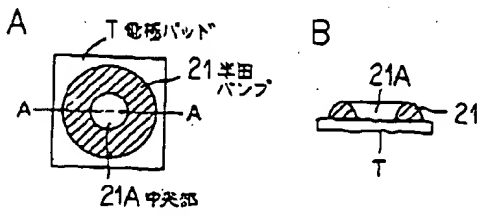
【図6】　図5に示した表面実装型スイッチを基板に表面実装する半田付け方法を示していて、同図Aは基板にこの発明の表面実装型スイッチを載置する状態を示した斜視図であり、同図Bは表面実装型スイッチが基板に半田付けされた状態を示した断面側面図である。

【図7】　従来技術のフリップチップ型ICの電極の構造及びそのフリップチップ型ICを基板に表面実装した場合の状態を示した側面図である。

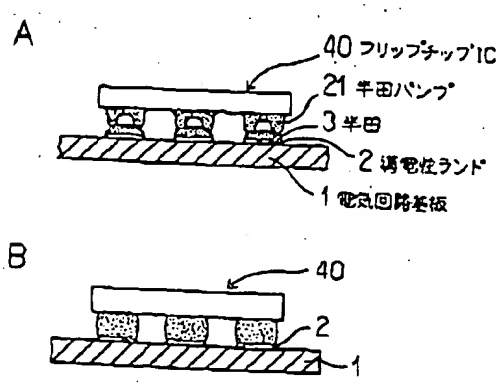
【符号の説明】

T　電極パッド
1　電気回路配線基板（基板）
2　導電性ランド
3　半田
21　断面凹状の半田バンプ
21A　断面台形状の半田バンプ
31　絶縁樹脂膜
34　半田
40　断面凹状の半田バンプを備えたフリップチップ型IC
40A　断面台形状の半田バンプを備えたフリップチップ型IC
50　表面実装型スイッチ
51　導電性端子
52　樹脂膜
53　断面凹状の半田バンプ

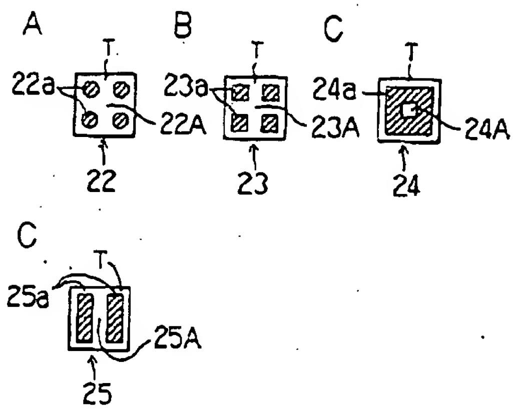
【図1】



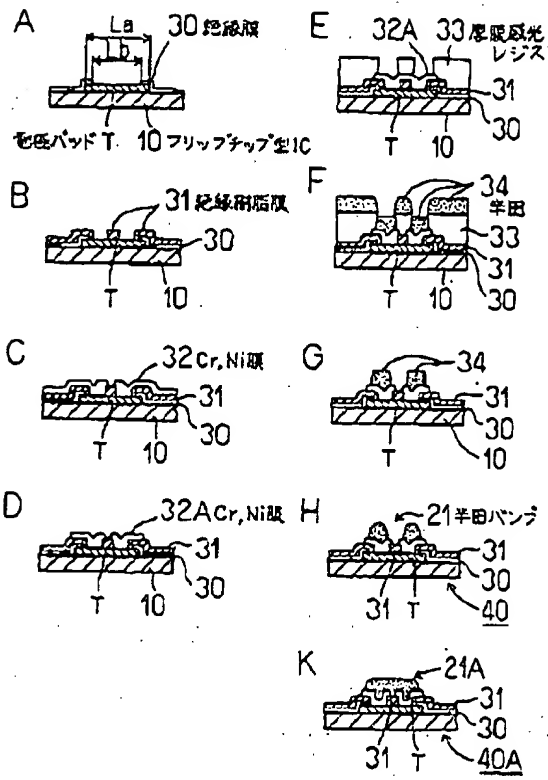
【図4】



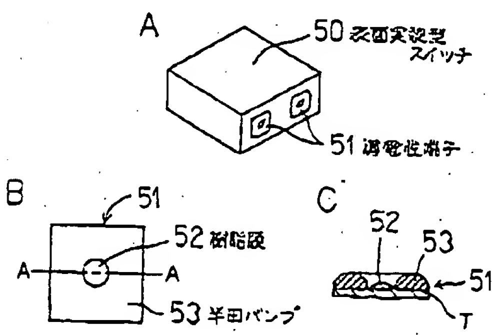
【図2】



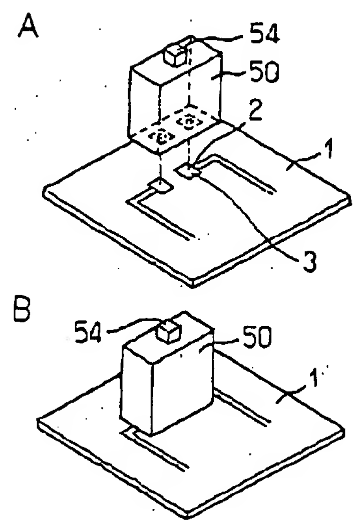
【図3】



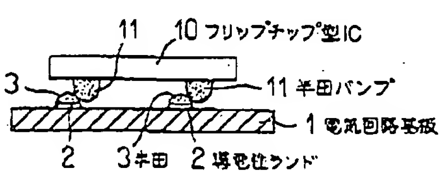
【図5】



【図6】



【図7】



1/1 - (C) PAJ / JPO

PN - JP7066207 A 19950310

PA - SONY CORP

I - H01L21/321 ; H01L21/60 ; H05K3/34

TI - SURFACE MOUNT DEVICE, MANUFACTURE THEREOF, AND SOLDERING METHOD

AB - PURPOSE:To solder a surface mount device to a circuit board without causing defective bonds by giving its electrodes solder bumps with a recess in the center so that they can seat on conductive projections on the board to correctly position the device.

- CONSTITUTION:A surface mount device has electrodes T each provided with a solder bump 21 having a recess in the center. For example, a ring-shaped solder bump 21 with a recess 21A in the center is formed on the electrode pad of a surface mount device, such as a flip chip IC. Such a device is mounted on a circuit board in such a manner that the recessed bumps seat on conductive projections on the board. Then, the surface mount device is soldered to the board by heating.